Karunya University
(Karunya Institute of Technology and Sciences)
(Declared as Deemed to be University under Sec.3 of the UGC Act, 1965)

End Semester Examinations - 2015-16 Even Semester - May 2016

14EC3025 CADfor VLSICircuits

Set A

Time : 3 hrs
Total Marks: 100

1. Draw the flow chart for new physical design cycle and explains its concepts in detail for CAD VLSI design?(20)

OR

2. a) Draw 'Y' chart for VLSI design tools and explain all the models in detail relevant to Computer aided design?(14)

b)List the difference between full custom design and semicustom design?(6)

3. Describe the depth first search algorithm and explain the same with the sample pseudo code for CAD VLSI design?(20)

OR

4. a) Define Vertex and Edge in Graph representation?(6)

b) Draw the data structure for the representation of graphs using an matrix format in CAD VLSI?(14)

5. Write the Shannon expression and explain the binary discuss diagram (BDD) in detail with an example? (20)

OR

6.

a) Explain gate level modeling and simulation with various types of representation in CAD VLSI?(14)

(b) What is Compaction? Explain in detail with an example?(6)

7. Describe the different design styles present in partitioning in VLSI and explain the same in detail?(20)

OR

8. a) What is mean by routing in CAD VLSI? List the two phases of routing in VLSI.(10)

b)Draw the flow diagram of two phases of routing and explain the same in detail?(10)

9. What is Physical design automation in FPGA? Explain the physical design automation steps in detail with neat diagrams?(20)

Wishing you All the Best